**Remarks:**

Reconsideration of the application, as amended herein, is respectfully requested.

Claims 1, 3 - 4, 6 - 7 and 9 are presently pending in the application. Claims 1, 4 and 7 have been amended. Claims 2, 5 and 8 were previously canceled.

Applicants would like to thank Examiner Parries and Examiner Deberadinis for the courtesy shown to Applicants' representative in a telephone interview of September 27, 2006, as well as in other telephone conversations with Examiner Parries.

In item 5 of the above-identified Office Action, claims 1, 3, 4, 6, 7, and 9 were rejected under 35 U.S.C. § 103(a) as allegedly being obvious over U. S. Patent No. 5,761,517 to Durham et al ("**DURHAM**") in view of U. S. Patent No. 5,943,203 to Wang ("**WANG**").

Applicants respectfully traverse the above rejections, as applied to the amended claims.

More particularly, Applicants' independent claims 1, 4 and 7 have been amended to recite, among other limitations:

> said control device **adjusting said clock frequency** to provide at said output, **at any time, the maximum possible clock frequency corresponding to a maximum permissible current consumption of the circuit.** [emphasis added by Applicants]

Applicants' amended claims are supported by the specification of the instant application, for example, by the last sentence of Applicants' Abstract of the Invention, which states:

> Such a **circuit ensures that a maximum permissible current consumption is not exceeded**, but, at the same time, **makes possible a maximum power of the circuit by a maximum clock frequency**. [emphasis added by Applicants]

See also, page 4 of the instant application, line 25 - page 5, line 7, which states:

> The circuit, thus, measures the instantaneous current consumption and, **based upon the latter, controls the frequency of the clock signal** with which the circuit configuration is supplied. **This ensures that the circuit configuration always operates with the maximum power that is possible taking account of the permissible maximum values for the current consumption.** Thus, the maximum possible power is always available, without the circuit configuration being endangered by excessively great heating. [emphasis added by Applicants]

That Applicants' clock frequency is set to a **maximum possible clock frequency for the maximum permissible current consumption, at any time** during the operation of the circuit, is supported by the specification of the instant application, for example, on page 7 of the instant application, lines 9 - 21, which states:

> When computational operations that have a high current demand are carried out in the circuit configuration 1, the demand is detected by the current measuring device 2 and, **provided that this results in exceeding the maximum permissible current, the control device 3 drives the clock supply circuit 4 such that the clock frequency made available to the circuit configuration 1 is reduced**. By virtue of the reduction in the clock frequency with which the circuit configuration 1 operates, the current consumption thereof also decreases, which decrease the measuring device 2 detects. **On account of this, the clock frequency provided by the clock circuit 4 is increased again so that, at any time, a maximum possible clock frequency is made available**. [emphasis added by Applicants]

As such, Applicants' specification specifically teaches, among other things, that Applicants' invention adjusts the clock frequency to **always** provide (i.e., **at any time** during the operation of the circuit) the **maximum possible clock frequency corresponding to the maximum permissible current consumption value.**

The **DURHAM** reference does **not** teach or suggest **adjusting the clock frequency such that the clock frequency provided, at any time**, is the **maximum possible clock frequency corresponding to the maximum permissible current consumption.** Rather, **DURHAM** discloses a state machine having different levels, wherein each level is associated with a predetermined clock pattern, as shown more particularly, in Fig. 2 of **DURHAM.** As will be described herebelow, contrary to Applicants' claimed invention, the system disclosed in **DURHAM** is unable to adapt

quickly to changing requirements, i.e. the instantaneous current consumption of an electronic circuit.

Col. 8 of **DURHAM**, lines 8 - 27 describe the process **DURHAM** uses to cycle through each of the clock frequency levels, as follows:

> Referring to FIG. 2, a state diagram is shown wherein level 4 is represented by reference numeral 104 and is the state of the system at initial power on (system clock speed equal to the oscillator clock). So long as the power--high signal is inactive, or low, the system will remain at the level 4 frequency. However, when the state machine 16 determines that the power--high signal is high the system steps to level 3 as shown by reference numeral 103. **So long as the power--high signal remains active, the system steps down through the various levels to level 2 (102), level 1 (101) and level 0 (100).** At level 0 so long as the power--high signal remains high (active), the system remains turned off at level 0, as previously discussed. **However, once the power--high signal becomes inactive then the system steps back up through the various state levels, i.e. level 1 (101), level 2 (102), level 3 (103) to level 4 (104).** For some applications, the present invention will seek out a specific level and remain at that level using the state of the power--high signal as feedback input to achieve dynamic adjustment of the system clock frequency. [emphasis added by Applicants]

As such, **DURHAM** discloses iteratively **stepping through the levels 4 - 0, instead of proceeding directly to the maximum possible clock frequency for the maximum permissible current consumption**, as required by Applicants' claims. That Applicants' claimed invention **proceeds directly to the maximum possible clock frequency** is emphasized by the recital that "**at**

**any time"** the clock frequency is the maximum possible clock frequency corresponding to the maximum permissible current consumption. Applicants' clock frequency is **always** (i.e., **"at all times"**) set to the **maximum possible clock frequency for the permissible current consumption.**

In contrast to Applicants' claimed invention, in the example of col. 8 of **DURHAM**, lines 8 - 18, there are at least four **"times"** in **DURHAM** when the clock frequency is **not** set to the maximum possible clock frequency for the maximum permissible current consumption. More particularly, in **DURHAM**, when the system is at level 4 frequency, and the power_high signal is **active**, the system of **DURHAM** steps the clock to the level 3 frequency, **without regard to whether the level 3 frequency is optimized for (i.e., the maximum possible clock frequency) the maximum permissible current consumption**, and, in fact, in the example of **DURHAM**, it is not. As shown in col. 8 of **DURHAM**, lines 15 - 18, the clock frequency has been adjusted to level 3 frequency, but the **power_high signal is still active.** As such, in **DURHAM, at this time** (i.e., level 3 frequency, power_high signal high) **the clock frequency is not the maximum possible clock frequency corresponding to the maximum permissible current consumption.** Rather, the clock frequency at level three of **DURHAM is too high for the circuit's current maximum permissible current consumption.**

As shown in col. 8 of **DURHAM**, lines 16 - 18, the system of **DURHAM** then reduces the clock frequency to the level two clock frequency, **regardless of whether the level two clock frequency is the optimal clock frequency for the maximum permissible current consumption of the circuit.** **DURHAM** again determines that the power_high signal is still active, in which case, again, **DURHAM** displays an instance (i.e., a "**time**") where **the clock frequency of DURHAM is not the maximum possible clock frequency corresponding to the maximum permissible current consumption.** Again, **the clock frequency of DURHAM at this time** (i.e., level two frequency, power_high signal active) **is too high for the circuit's current maximum permissible current consumption.**

**DURHAM** even discloses prolonging these periods of time when the clock frequency is **not** the maximum possible clock frequency corresponding to the maximum permissible current consumption. For example, col. 6 of **DURHAM**, lines 53 - 57, state:

> Control state machine 16 will then continually monitor latch 15 and **if the power_high signal is still present after a predetermined amount of time**, select signals will be provided to pattern generator 17 which **will cause the present invention to move to state level 2.** [emphasis added by Applicants]

Thus, not only are there times when the system of **DURHAM** has not optimized the clock frequency for the maximum permissible current consumption, as required by Applicants' claims, but **DURHAM** discloses purposely **waiting** in this state until after **"a predetermined amount of time"** to move to the next stage, which may, or may not, render the power_high signal inactive. Further, the same process described in connection with levels 2 and 3 of **DURHAM** are repeated as **DURHAM steps through** the clock frequencies of levels 1 and 0. As described above, this **stepping** process, (i.e., the iterative adjustment) of **DURHAM** produces **times** where **the clock frequency** of the circuit **is not the maximum possible clock frequency corresponding to the maximum permissible current consumption.**

Consequently, in the above illustrative example taken directly from the specification of **DURHAM**, in the system of **DURHAM at least four measurement periods have to lapse** before **DURHAM** provides a clock signal with the maximum clock rate corresponding to the maximum permissible current consumption. This is in stark contrast to Applicants' invention, in which a clock signal is adjusted to provide, **at all times**, the maximum possible clock frequency corresponding to the maximum permissible current consumption.

This stepping process of **DURHAM** additionally occurs in the reverse direction (i.e., when stepping back up to level four clock frequency), as disclosed in col. 8 of **DURHAM**, lines 20 - 23 (i.e,. "However, once the power_high signal becomes inactive then the system **steps back up through the various state levels**, i.e. level 1 (101), level 2 (102), level 3 (103) to level 4 (104)"). Thus, as the clock frequency is returned to the level four clock frequency, once the power_high signal is inactive, **DURHAM** discloses **stepping through each of the clock frequency levels irregardless of whether that clock frequency level provides the maximum possible clock frequency corresponding to the maximum permissible current consumption**, and, as such, is not providing the **maximum possible clock frequency corresponding to the maximum permissible current consumption at all times**, as required by Applicants' claims.

As a result of the disclosed stepping up and down through the frequency levels of **DURHAM**, the system of **DURHAM** does not **operate using the maximum power values possible taking into account the maximum permissible current consumption of the circuit**, and thus, at times, either under utilizes the circuit (i.e., while stepping up through the levels), or risks overheating the circuit (i.e., while stepping down through the levels).

Further, Applicants' believe that the clock generator disclosed in **DURHAM** isn't even capable of maximizing the clock frequency corresponding to the maximum permissible current consumption, **at all times**, as required by Applicants' claimed invention. **DURHAM** clearly teaches using a **pattern generator to input a digital signal to a series of interconnected registers which make up a loadable shift register.** See, for example, the Abstract of **DURHAM**, which states, in part:

> A pattern generator is used to input a digital signal to a series of interconnected registers which make up a loadable shift register. The output of the pattern generator is based upon the input from the sensor. **The bits shifted through the shift register are ANDed with the oscillator clock signal to control the frequency of the system clock.** [emphasis added by Applicants]

See also, col. 5 of **DURHAM**, line 61 - col. 7, line 26. By using a **fixed pattern** to remove clock pulses having a close relationship to one another, for example, every fourth clock pulse (i.e., see col. 6 of **DURHAM**, lines 46 - 52), **cannot be used to achieve the objective of the presently claimed invention** (i.e., to, **at all times**, provide the maximum possible clock rate).

The **WANG** reference, cited in the Office Action in combination with **DURHAM** for allegedly disclosing an instantaneous current sensor, does not cure the above-discussed deficiencies of the **DURHAM** reference. Rather, a person of ordinary skill in the

art trying to combine the teachings of **DURHAM** with the teachings of **WANG**, in the manner argued in the Office Action, would, arguendo, merely produce a circuit as disclosed by **DURHAM** with an instantaneous current sensor as disclosed by **WANG**. However, even if sensing of the current consumption of **DURHAM**'s electronic circuit were instantaneous, the circuit stepping through the levels in the process disclosed by Durham would not be instantaneous, as discussed above. Thus, even when combining the teachings of **DURHAM** and **WANG**, arguendo, the combination would not teach, suggest or motivate a person of ordinary skills in this art to make Applicants' currently claimed invention.

Thus, Applicants' currently claimed invention is believed to be patentable over **DURHAM** and **WANG**, taken alone, or in combination.

Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion or motivation to do so **found either in the references themselves or in the knowledge generally known by one of ordinary skill in the art of the invention**. Applicants believe that there is no motivation to combine **DURHAM** with **WANG**. More particularly, Applicants believe that **WANG** is not relevant to the particular problem with which the applicant was concerned. Like **DURHAM**,

**WANG** does not teach or suggest adapting an output clock frequency instantaneously, such that the output clock frequency is **at all times** optimized to the maximum permissible current consumption. Rather, **WANG** discloses a circuit capable of measuring an instantaneous current. This, however, is not pertinent to the particular problem with which the applicant was concerned at the time the invention was made.

In view of the foregoing, Applicants' currently claimed invention is believed to be patentable over **DURHAM** and **WANG**, taken alone, or in any combination.

It is accordingly believed that none of the references, whether taken alone or in any combination, teach or suggest the features of claims 1, 4 and 7. Claims 1, 4 and 7 are, therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on claims 1, 4 or 7.

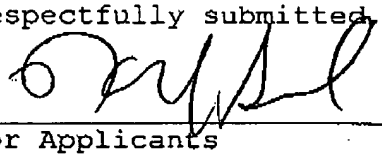
In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out. In the alternative, the entry of the amendment is requested, as it is believed to place the application in

better condition for appeal, without requiring extension of the field of search.

The instant Amendment is being filed simultaneously with a Request for Continuing Examination (RCE) and its associated fee. If an extension of time for this paper is required, petition for extension is herewith made.

Please charge any additional fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,



Kerry P. Sisselman
Reg. No. 37,237

For Applicants

September 27, 2006

Lerner Greenberg Stemer LLP
Post Office Box 2480
Hollywood, FL 33022-2480
Tel: (954) 925-1100
Fax: (954) 925-1101